Low Noise, Low Drift, Low Power 3-Axis Accelerometer

PRELIMINARY

ADXL354/ADXL355

FEATURES

- Hermetic package offers excellent long-term stability
- Offset temperature coefficient of <0.15m*g*/°C (max) with minimal hysteresis
- Ultralow noise density: 25µg/√Hz
- Low power:
  - 200 µA in measurement mode (digital)
  - 175 µA in measurement mode (analog)
  - 30 µA in standby mode
- Digital SPI/I²C interfaces
  - 20-Bit ADC
  - Data interpolation routine for synchronous sampling
  - Programmable high- and low-pass filters
- Analog interface
  - Bandwidth set with external capacitor
- Electromechanical self-test
- Integrated temperature sensor
- Supply voltage options:
  - 2.25 V to 3.6 V with internal regulators
  - Or 1.8 V ± 10%
- Operating Temperature Range: -40°C to 125°C
- 6 mm × 6 mm × 2.1 mm 14-pin hermetic, 0.26grams ceramic package

APPLICATIONS

- IMU/AHRS
- Stabilization systems
- Structural Health Monitoring
- Seismic imaging
- Tilt sensing
- Robotics
- Condition Monitoring

GENERAL DESCRIPTION

The ADXL354 (analog output) ADXL355 (digital output) are low noise density, low 0-g offset drift, low power, 3-axis accelerometers with selectable measurement ranges up to ±8 *g*. The ADXL354/355 offer industry-leading noise, temperature and long-term stability in the application with minimal calibration.

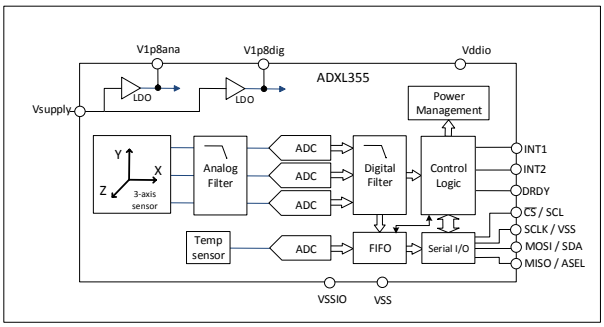

Figure 1: ADXL355 Functional Block Diagram.

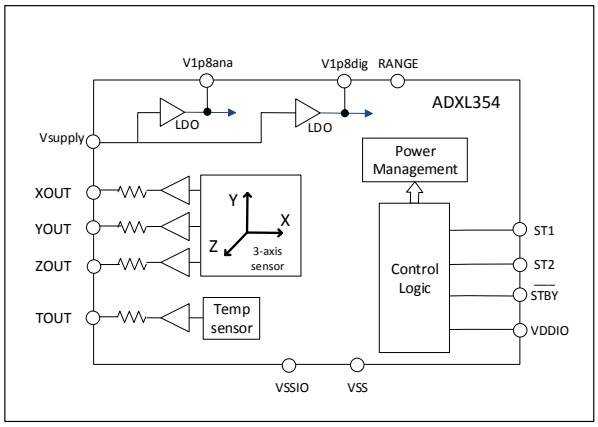

Figure 2: ADXL354 Functional Block Diagram.

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Low Noise, Low Drift, Low Power 3-Axis Accelerometer

PRELIMINARY

ADXL354/ADXL355

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Specifications ... 4
Absolute Maximum Ratings ... 10
ESD caution ... 10
Acceleration Sensitive AxEs ... 10
Pin Configuration and Function Descriptions ... 11
Typical Performance Charts ... 13
ADXL 354 (Analog output) ... 13
ADXL 355 (DIGITAL output) ... 14
Application Information ... 16
Theory of Operation ... 16
Digital Output ... 16
Analog Output ... 16
Power Sequencing ... 17
Power Supply Description ... 17
Over-Range Protection ... 17
Self Test ... 17
Serial Communication ... 21
SPI Protocol ... 21
I2C Protocol ... 23
Reading Acceleration or Temperature Data from the Interface ... 23
FIFO ... 24
Interrupts ... 25
External Sync and Interpolation ... 25
ADXL355 Register Map ... 29
Register Definitions ... 31
Analog Devices ID Register ... 31
Analog Devices MEMS ID Register ... 31
Device ID Register ... 31
Product Revision ID Register ... 31
Status Register ... 31
FIFO Entries Registers ... 32
Temperature Data Registers ... 32
X-Axis Data Registers ... 32
Y-Axis Data Registers ... 33
Z-Axis Data Registers ... 33
FIFO Access Register ... 34
X-Axis Offset Trim Registers ... 34
Y-Axis Offset Trim Registers ... 34
Z-Axis Offset Trim Registers ... 35
Activity Enable Register ... 35
Activity Threshold Registers ... 35
Activity Count Register ... 36
Filter Settings Register ... 36
FIFO Samples Register ... 36
Interrupt Pin Function Map Register ... 37
Data Synchronization ... 37
I2C Speed, Interrupt Polarity and Range Register ... 37
Power Control Register ... 38
Self-Test Register ... 38
Reset Register ... 38
Recommended Soldering Profile ... 39
PCB Footprint Pattern ... 40
Outline Dimensions ... 41
Ordering Guide ... 41

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Low Noise, Low Drift, Low Power 3-Axis Accelerometer

PRELIMINARY

ADXL354/ADXL355

SPECIFICATIONS

T_A = 25°C, V_{SUPPLY} = 3.3 V, acceleration = 0 *g*, Output Data Rate = 125Hz.

Table 1: ADXL355 (DIGITAL OUTPUT)

Parameter	Test Conditions	Min[2]	Typ[1]	Max	Unit
SENSOR INPUT	Each axis				
Output Full Scale Range (FSR)	User selectable		±2.048		*g*
			±4.096		
			±8.192		
Nonlinearity[1]	±2*g*		0.1		%
Cross-Axis Sensitivity			1		%
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±2 *g*	235520	256000	276480	LSB/*g*
	±4 *g*	117760	128000	138240	LSB/*g*
	±8 *g*	58880	64000	69120	LSB/*g*
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	±2 *g*		3.9		µ*g*/LSB
	±4 *g*		7.8		µ*g*/LSB
	±8 *g*		15.6		µ*g*/LSB
Sensitivity Change Due to Temperature	-40°C to 105°C		±0.01		%/°C
Sensitivity Change Due to Temperature	-40°C to 125°C		±TBD		%/°C
Repeatability[Error! Bookmark not defined.]			±TBD		%
0 *g* OFFSET	Each axis, ±2 *g*				
0 *g* Output for X_{OUT}, Y_{OUT}, Z_{OUT}		−150	±25	+150	m*g*
0 *g* Offset vs. Temperature (XYZ axes)[2]	-40°C to 105°C	−0.15	±0.02	0.15	m*g*/°C
0 *g* Offset vs. Temperature (XYZ axes)	-40°C to 125°C	−TBD	±TBD	TBD	m*g*/°C
Repeatability[3]			±5		m*g*
Vibration Rectification	±8 *g* range, offset shift under 2.5g rms 50Hz to 2kHz random vibration, 4kHz ODR		<0.4		g
NOISE	±2 *g*				
X, Y, Z Axes			25		µ*g*/√Hz
Velocity Random Walk			TBD		µm/s/√hr
OUTPUT DATA RATE AND BANDWIDTH	User Selectable				
Bandwidth					
Low Pass Filter -3 dB Frequency			1 … 1000		Hz

[1] The typical specifications shown are for at least 68% of the population of parts and are based on the worst case of mean ±1 σ, except for sensitivity, which represents the target value.

[2] Min/Max is determined by characterization and represents 99.97% of the population.

[3] Includes shifts due to HTOL (T_A = 150°C, V_S = 3.6V, 1000hrs) and Temperature Cycling (-55°C to 125°C, 1000 cycles).

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Parameter	Test Conditions	Min[2]	Typ[1]	Max	Unit
High Pass Filter -3 dB Frequency			DC … 10		Hz
Output Data Rate to Bandwidth Ratio			4		
SELF-TEST					
Output Change in X-Axis			0.3		*g*
Output Change in Y-Axis			0.3		*g*
Output Change in Z-Axis			1.5		*g*
POWER SUPPLY					
Operating Voltage Range (V_{SUPPLY})		2.25	2.5	3.6	V
I/O Voltage Range ($V_{DDI/O}$)		V1p8dig	2.5	3.6	V
Operating Voltage with Internal LDO bypassed	V_{SUPPLY} = 0V	1.62	1.8	1.98	V
Supply Current			200		µA
Standby Mode Current			30		µA
Turn-On Time	Standby to measurement mode (to within 1mg of final value, 2g range)		<10		ms
	Power-off to standby		<10		ms
TEMPERATURE SENSOR					
Output at 25°C			1852		LSB
Long term stability[3]			TBD		°C
Scale Factor			-9.05		LSB/°C
TEMPERATURE					
Operating Temperature Range		–40		+125	°C

$T_A = 25°C$, $V_{SUPPLY} = 3.3$ V, acceleration = 0g.

Table 2: ADXL354 (ANALOG OUTPUT)

Parameter	Test Conditions	Min	Typ[1]	Max	Unit
SENSOR INPUT	Each axis				
Output Full Scale Range (FSR)	ADXL354B		±2, ±4		*g*
	ADXL354C		±2, ±8		*g*
Nonlinearity[1]	±2 *g*		0.1		%
Cross-Axis Sensitivity			1		%
SENSITIVITY	Ratiometric to V1p8ana				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	±2 *g*	368	400	432	mV/g
	±4 *g*	184	200	216	mV/g
	±8 *g*	92	100	108	mV/g
Sensitivity Change Due to Temperature	-40°C to 105°C		±0.01		%/°C
Sensitivity Change Due to Temperature	-40°C to 125°C		±TBD		%/°C
Repeatability[3]			TBD		%
0 *g* OFFSET	Each axis, ±2 *g*				
0 *g* Output for X_{OUT}, Y_{OUT}, Z_{OUT}	Referred to V1p8ana/2	−150	±25	+150	m*g*
0 *g* Offset vs. Temperature (XYZ axes)[Error! Bookmark not defined.]	-40°C to 105°C	−0.15	±0.1	0.15	m*g*/°C
0 *g* Offset vs. Temperature (XYZ axes)[Error! Bookmark not defined.]	-40°C to 125°C	−TBD	±TBD	TBD	m*g*/°C
Repeatability[Error! Bookmark not defined.]			±5		m*g*
Vibration Rectification	±8 *g* range, offset shift under 2.5g rms 50Hz to 2kHz random vibration, 4kHz ODR		<0.4		g
NOISE	±2 *g*				
X, Y, Z Axes			25		µg/√Hz
Velocity Random Walk			TBD		µm/s/√hr
BANDWIDTH					
LPF ±3 dB Frequency	Set by external capacitors		1 … 1000		Hz
SELF-TEST					
Output Change in X-Axis			0.3		*g*
Output Change in Y-Axis			0.3		*g*
Output Change in Z-Axis			1.5		*g*
POWER SUPPLY					
Operating Voltage Range (V_{SUPPLY})		2.25	2.5	3.6	V
I/O Voltage Range ($V_{DDI/O}$)		V1p8dig	2.5	3.6	V
Operating Voltage with Internal LDO bypassed	V_{SUPPLY} = 0V	1.62	1.8	1.98	
Supply Current			175		µA
Turn-On Time	Standby to measurement mode (to within		<10		ms

[1] The typical specifications shown are for at least 68% of the population of parts and are based on the worst case of mean ±1 σ, except for sensitivity, which represents the target value.

[2] Min/Max is determined by characterization and represents 99.97% of the population.

[3] Includes shifts due to HTOL (T_A = 150°C, V_S = 3.6V, 1000hrs) and Temperature Cycling (-55°C to 125°C, 1000 cycles).

Parameter	Test Conditions	Min	Typ[1]	Max	Unit
	1mg of final value, 2g range)				
	Power-off to standby		<10		ms
OUTPUT AMPLIFIER					
Swing	No load	0.03		V1p8ana – 0.03	V
Output Resistance			32		kΩ
TEMPERATURE SENSOR					
Output at 25°C			892.2		mV
Long term stability[3]			TBD		°C
Scale Factor			3.0		mV/°C
TEMPERATURE					
Operating Temperature Range		−40		+125	°C

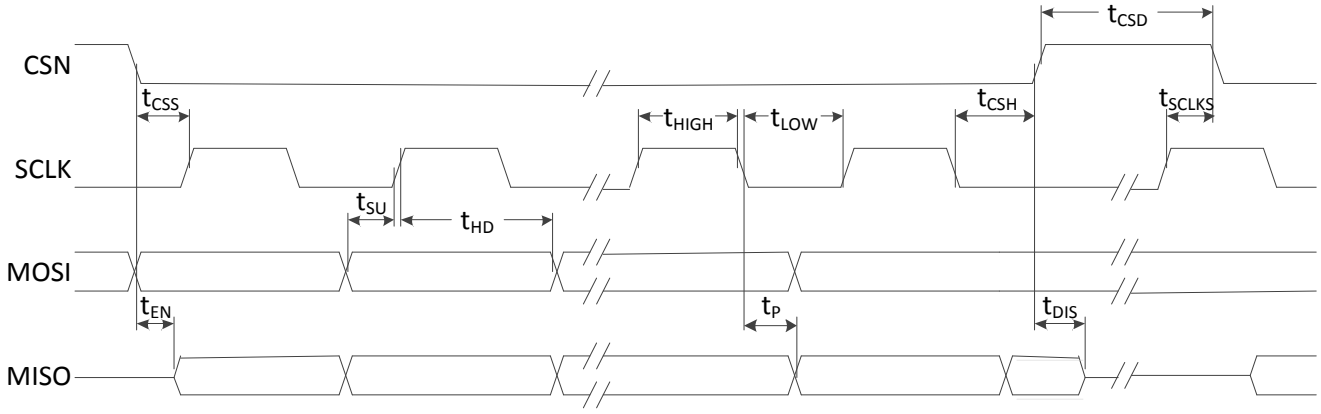

Figure 3 SPI Interface Timing Parameters

Table 3 ADXL355 SPI DIGITAL INTERFACE CHARACTERISTICS

Parameter	Description	Min	Typ[1]	Max	Unit
INPUT DC LEVELS					
V_{IL}	Low level input voltage			0.3*V_{DDIO}	V
V_{IH}	High level input voltage	0.7*V_{DDIO}			V
I_{IL}	Low level input current, V_{IN}=0V	-0.1			µA
I_{IH}	High level input current, V_{IN}=V_{DDIO}			0.1	µA
OUTPUT DC LEVELS					
V_{OL}	Low level output voltage, I_{OL}=$I_{OL,Min}$			0.2*V_{DDIO}	V
V_{OH}	High level output voltage, I_{OL}=$I_{OH,Max}$	0.8*V_{DDIO}			V
I_{OL}	Low level output current, V_{OL}=$V_{OL,Max}$	-10mA			mA
I_{OH}	High level output current, V_{OL}=$V_{OH,Min}$			4mA	mA
INPUT AC Parameters					
SCLK Frequency		0		10	MHz
t_{HIGH}	SCLK high time	40			nsec
t_{LOW}	SCLK low time	40			nsec
t_{CSS}	CSN set-up time	20			nsec
t_{CSH}	CSN hold time	20			nsec

Parameter	Description	Min	Typ[1]	Max	Unit
t_{CSD}	CSN disable time	40			nsec
t_{SCLKS}	Rising SCLK setup time	20			nsec
t_{SU}	MOSI setup time	20			nsec
t_{HD}	MOSI hold time	20			nsec
OUTPUT AC Parameters					
t_P	Propagation delay, C_{LOAD}=30pF			30	nsec
t_{EN}	Enable MISO time	30			nsec
t_{DIS}	Disable MISO time			20	nsec

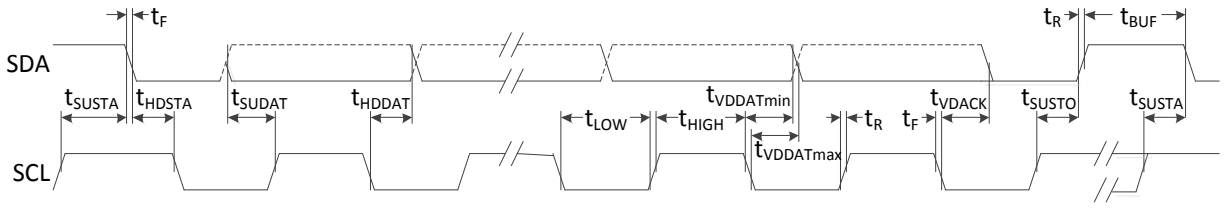

Figure 4 I2C Interface Timing Parameters

Table 4 I2C DIGITAL INTERFACE CHARACTERISTICS

		I2C_HS=0			I2C_HS=1			
Parameter	**Description**	**Min**	**Typ[1]**	**Max**	**Min**	**Typ[2]**	**Max**	**Unit**
INPUT DC LEVELS								
V_{IL}	Low level input voltage			0.3*V_{DDIO}			0.3*V_{DDIO}	V
V_{IH}	High level input voltage	0.7*V_{DDIO}			0.7*V_{DDIO}			V
V_{HYS}	Hysteresis of Schmitt trigger inputs	0.05*V_{DDIO}			0.1*V_{DDIO}			µA
I_{IL}	Input current, 0.1xV_{DDIO} <V_{IN}<0.9 xV_{DDIO}	-10		10				µA
OUTPUT DC LEVELS								
V_{OL1}	Low level output voltage, I_{OL}=3mA, V_{DD}>2V			0.4				V
V_{OL2}	Low level output voltage, I_{OL}=3mA, V_{DD}<=2V			0.2*V_{DDIO}				V
I_{OL}	Low level output current, V_{OL}=0.4V	20mA						mA
	Low level output current, V_{OL}=0.6V	6mA						mA
INPUT AC Parameters								
SCLK Frequency		0		1	0		3.4	MHz
t_{HIGH}	SCLK high time	260			60			nsec
t_{LOW}	SCLK low time	500			160			nsec
t_{SUSTA}	Start set-up time	260			160			nsec
t_{HDSTA}	Start hold time	260			160			nsec
t_{SUDAT}	Data set-up time	50			10			nsec
t_{HDDAT}	Data hold time	0			0			nsec

		I2C_HS=0			I2C_HS=1			
Parameter	**Description**	**Min**	**Typ[1]**	**Max**	**Min**	**Typ[2]**	**Max**	**Unit**
t_{SUSTO}	Stop setup time	260			160			nsec
t_{BUF}	Bus free time	500			-			nsec
t_{RCL}	SCL input rise time			120			160	nsec
t_{FCL}	SCL input fall time			120			80	nsec
t_{RDA}	SDA input rise time			120			160	nsec
t_{FDA}	SDA input fall time			120			160	nsec
t_{SP}	Width of spikes to be supressed			50			10	nsec
OUTPUT AC Parameters								
t_{VDDAT}	Data propagation delay, C_{LOAD}=550pF?	97		450	27		135	nsec
t_{VDACK}	ACK propagation delay, C_{LOAD}=550pF?			450			-	nsec
t_F	Output fall time	20x(V_{DD}/5.5)		120			TBD	nsec

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	TBD
Acceleration (Any Axis, Powered, 0.5 ms)	TBD
V_{SUPPLY}, V_{DDIO}	3.6 V
All other pins	TBD
Output Short-Circuit Duration (Any Pin to Common)	TBD
Operating Temperature Range	−40°C to +125°C
Storage Temperature	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification (Table 1, Table 2) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ACCELERATION SENSITIVE AXES

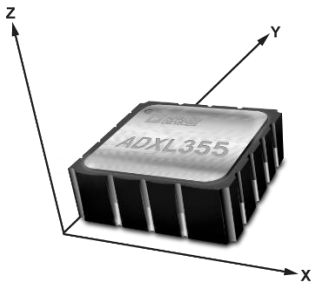

Figure 5. Axes of Acceleration Sensitivity (Corresponding Output Voltage Increases When Accelerated Along the Sensitive Axis)

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

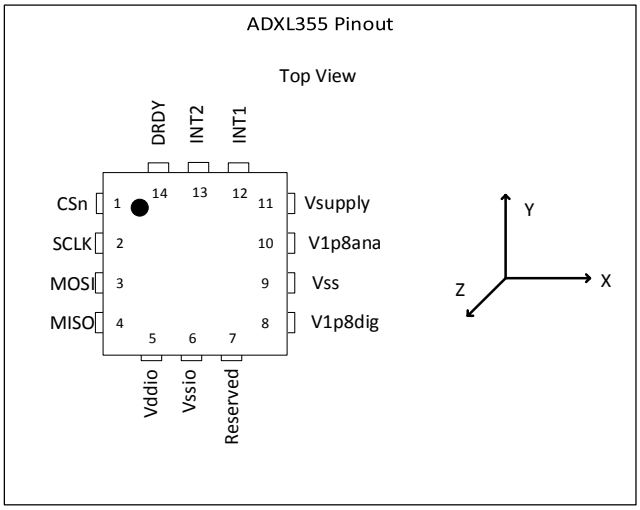

Figure 6. ADXL355 Pin Configuration (top view)

Table 6: ADXL355 Pin Function Descriptions

Pin No.	Pin Name	Description
1	CSn/SCL	SPI: Chip Select I2C: Serial Communications Clock
2	SCLK/Vssio	SPI: Serial Communications Clock I2C: Connect to Vssio
3	MOSI/SDA	SPI: Master Output Slave Input I2C: Serial Data
4	MISO/ASEL	SPI: Master Input Slave Output I2C: Alternate I2C Address Select
5	Vddio	Digital Interface Supply Voltage
6	Vssio	Digital Ground
7	Reserved	This pin can be connected to ground or left open
8	V1p8dig	Internal Logic supply. Needs bypass cap. Must be driven if Vsupply is connected to Vss.
9	Vss	Analog ground
10	V1p8ana	Analog supply. Needs bypass cap. Must be driven if Vsupply is connected to Vss.
11	Vsupply	2.25 - 3.6V For Vdd = 2.25-3.6V, V1p8dig, V1p8ana are regulator outputs For Vdd = 0V, V1p8dig, V1p8ana are 1.62-1.98V supply inputs
12	INT1	Interrupt Pin
13	INT2	Interrupt Pin
14	DRDY	Interrupt Pin

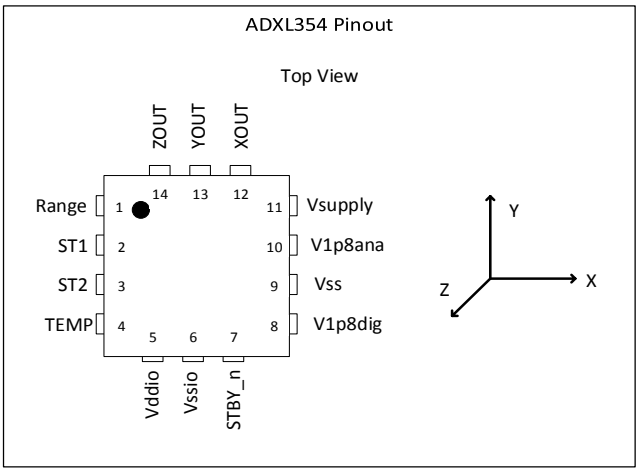

Figure 7. ADXL354 Pin Configuration (top view)

Table 7: ADXL354 Pin Function Descriptions

Pin No.	Pin Name	Description
1	Range	Range Selection Pin Set to ground to select ±2*g* range Set to Vddio to select ±4*g* or ±8*g* range (model dependent. See ordering guide)
2	ST1	Self-Test Pin
3	ST2	Self-Test Pin
4	Tout	Temperature Sensor Output
5	Vddio	Digital Interface Supply Voltage
6	Vssio	Digital Ground.
7	STBY_n	Select standby or measurement mode Set to ground to enter standby mode Set to Vddio to enter measurement mode
8	V1p8dig	Internal Logic supply. Needs bypass cap. Must be driven if Vsupply is connected to Vss.
9	Vss	Analog Ground
10	V1p8ana	Analog supply. Needs bypass cap. Must be driven if Vsupply is connected to Vss.
11	Vsupply	2.25 - 3.6V For Vsupply = 2.25-3.6V, V1p8dig, V1p8ana are regulator outputs. For Vsupply = 0V, V1p8dig, V1p8ana are 1.62-1.98V supply inputs.
12	Xout	X-axis output
13	Yout	Y-axis output
14	Zout	Z-axis output

TYPICAL PERFORMANCE CHARTS

ADXL 354 (ANALOG OUTPUT)

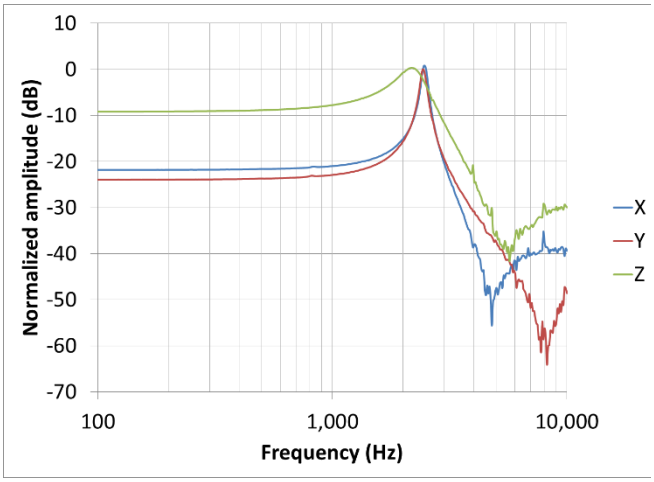

Figure 8 Frequency response of the sensor

ADXL 355 (DIGITAL OUTPUT)

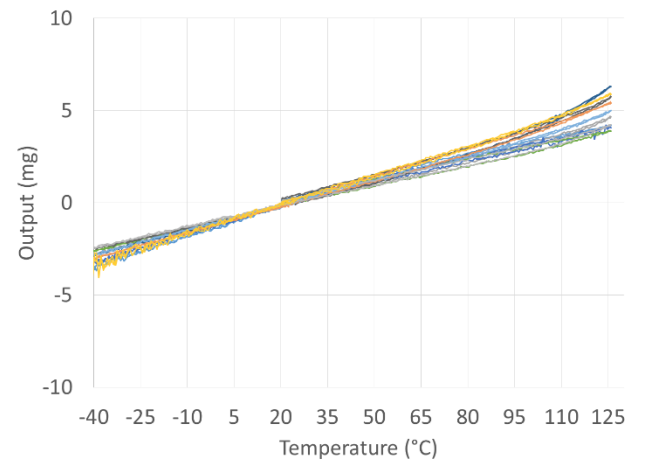

Figure 9 X-Axis offset vs temperature (N=15)

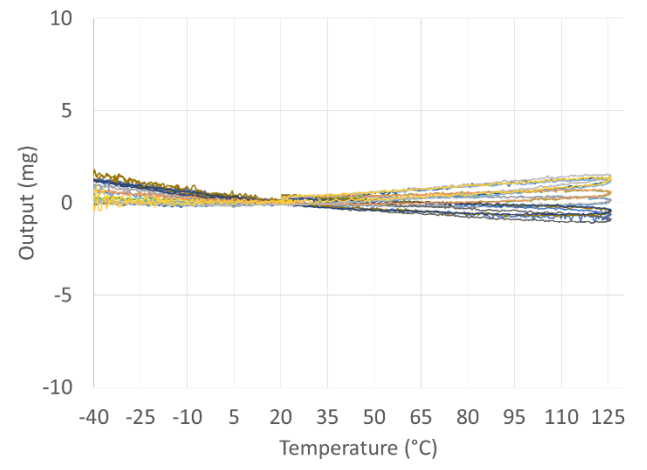

Figure 10 Y-Axis offset vs temperature (N=15)

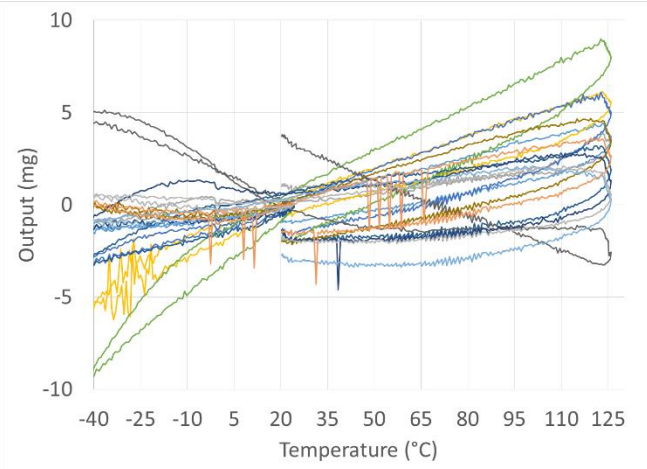

Figure 11 Z-Axis offset vs temperature (N=15)

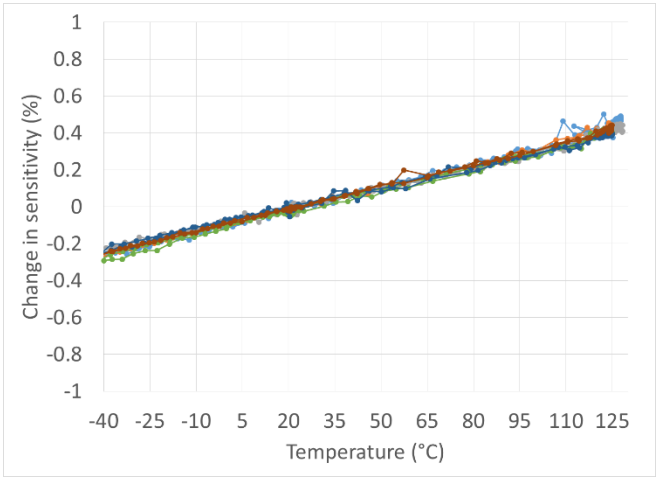

Figure 12 X-Axis sensitivity vs temperature

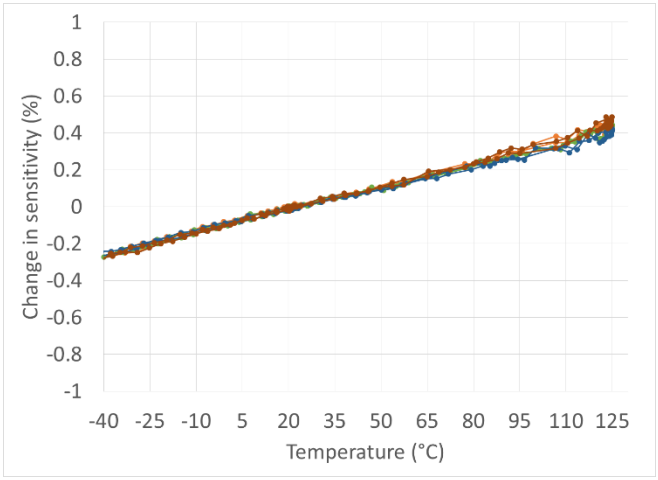

Figure 13 Y-Axis sensitivity vs temperature

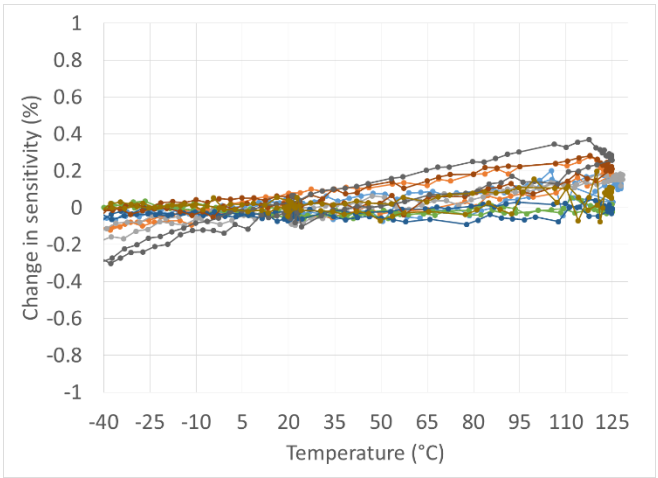

Figure 14 Z-Axis sensitivity vs temperature

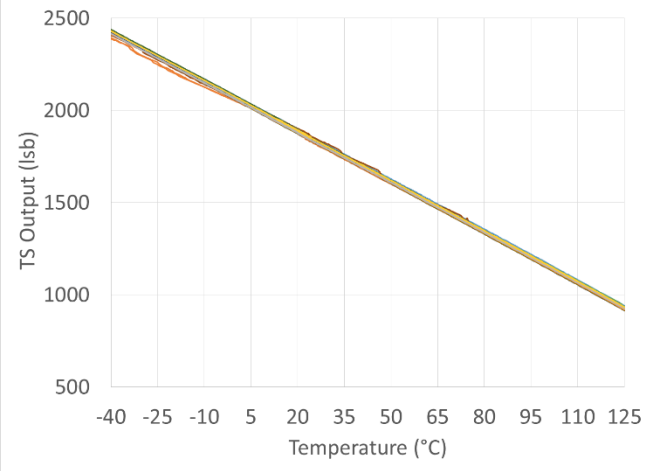

Figure 15 Temperature sensor output vs temperature (N=15)

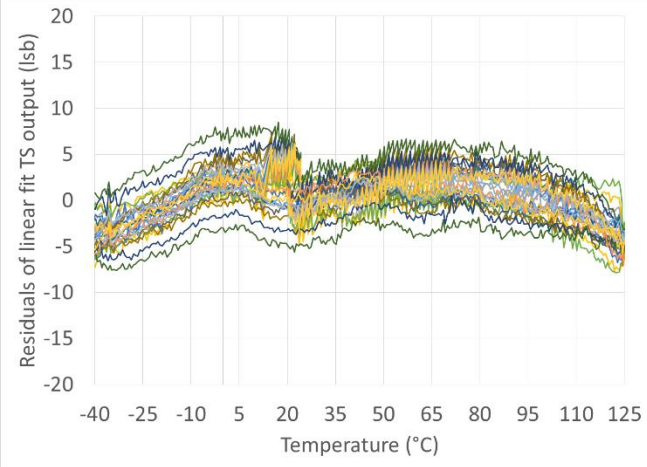

Figure 16 Residuals of linear fit to temperature sensor output vs temperature (N=15)

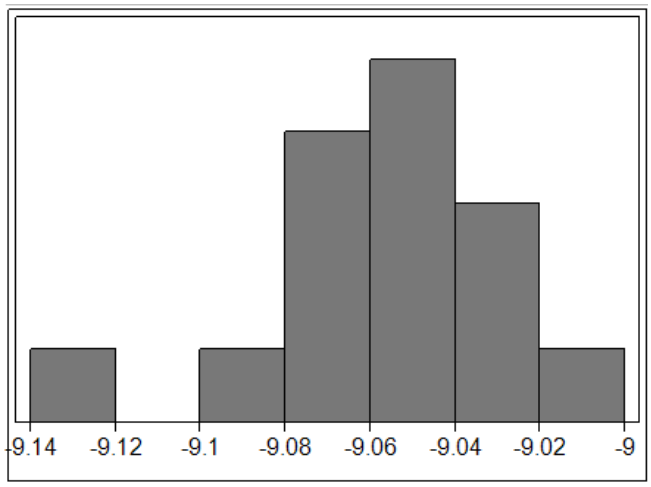

Figure 17 Temperature sensor scale factor in LSB/°C (N=15)

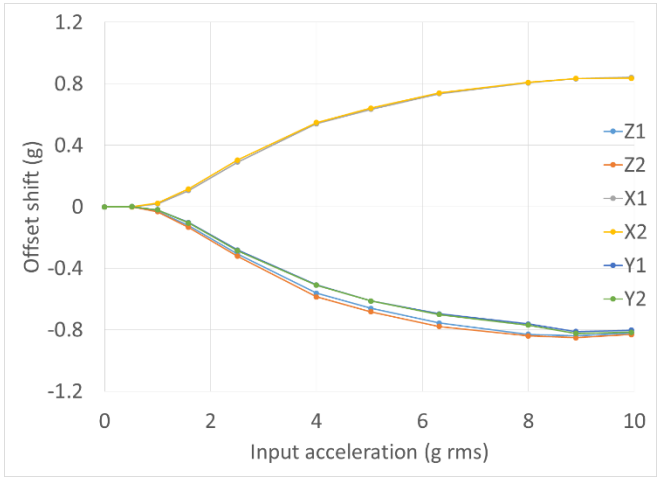

Figure 18 Vibration rectification in 2g range, 50Hz to 2kHz random vibration, 4kHz ODR

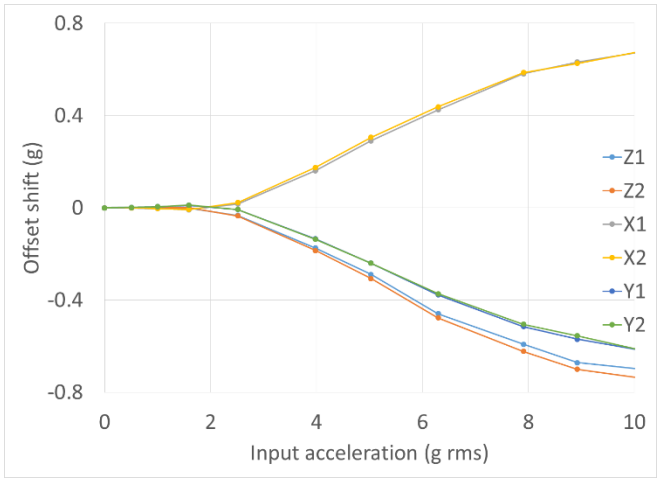

Figure 19 Vibration rectification in 4g range, 50Hz to 2kHz random vibration, 4kHz ODR

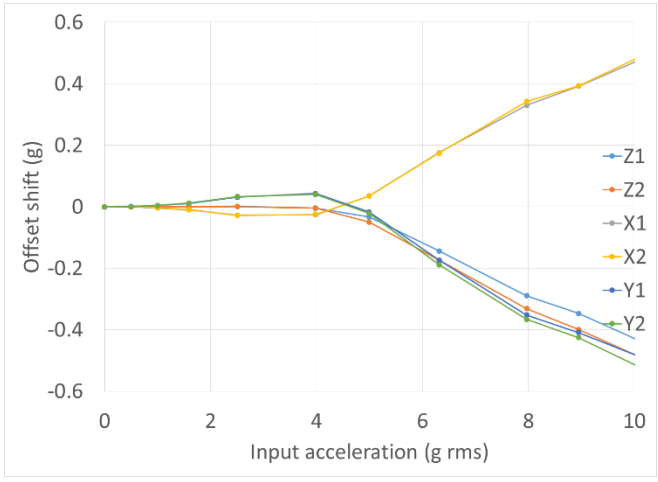

Figure 20 Vibration rectification in 8g range, 50Hz to 2kHz random vibration, 4kHz ODR

APPLICATION INFORMATION

THEORY OF OPERATION

The ADXL354 is a complete 3-axis ultra-low noise and ultra-stable offset accelerometer with outputs ratiometric to the analog 1.8V supply. The ADXL355 adds three high resolution ADCs which use the analog 1.8V supply as a reference to provide digital outputs insensitive to supply voltage. The ADXL354B is pin-selectable for ±2g or ±4g full scale, and the The ADXL354C is pin-selectable for ±2g or ±8g full scale. The ADXL355 is programmable for ±2g, ±4g or ±8g full scale. The ADXL355 offers both SPI and I2C communications ports.

The surface-micromachined sensing elements are fully differential, comprising lateral XY-axis sensors and vertical teeter-totter Z-axis sensors. The XY sensors and the Z sensors go through separate signal paths, which have been designed to minimize offset drift and noise. The signal path is fully differential, except for a differential to single-ended conversion at the analog outputs.

The analog accelerometer outputs of the ADXL354 are ratiometric to V1p8ana, so careful attention must be taken to digitize them correctly. The temperature sensor output is not ratiometric. All analog outputs include an internal 32kΩ resistor which can be used with a user-supplied external capacitor to set the bandwidth of the anti-alias filter.

The ADXL355 includes appropriate anti-alias filters before the ADC. User selectable output data rates and filter corners are provided. The temperature sensor is digitized with a 12-bit SAR converter.

DIGITAL OUTPUT

The ADXL355 application circuit is shown in Figure 21 with the recommended bypass capacitors. The communications interface is either SPI or I2C. See Serial Communication section for further details.

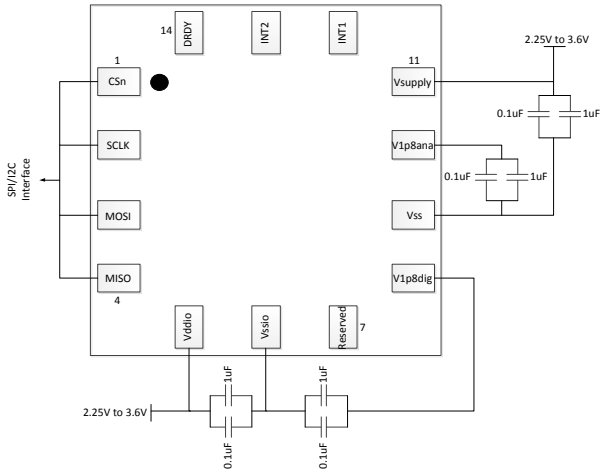

Figure 21. ADXL355 Application Circuit

The ADXL355 includes an internal configurable band-pass filter. Both the high- and low-pass poles of the filter are adjustable as shown in the Register Definition section under Filter Settings register. At power-up, the default condition for the filters is HPF = DC and LPF = 1000 Hz.

ANALOG OUTPUT

The ADXL354 application circuit is shown in Figure 22. The analog outputs (XOUT, YOUT and ZOUT) are ratiometric to the internal regulator voltage (V1p8ana) and need to be read carefully in order to achieve the product's inherent noise performance. The zero-*g* bias output is nominally equal to V1p8ana / 2. The recommended option is to use ADXL354 with a ratiometric ADC (e.g. Analog Devices AD7682) with V1p8ana providing the voltage reference. This configuration would result in self-cancellation of errors due to minor supply variations.

The ADXL354 outputs also include 32 kΩ resistance in series which can be used in conjunction with external capacitors to implement low-pass filtering for anti-aliasing and noise reduction. The anti-alias filter cutoff frequency should be significantly higher than the desired signal bandwidth. If the anti-alias filter corner is too low, then ratiometricity may be degraded where the signal attenuation is different than the reference attenuation.

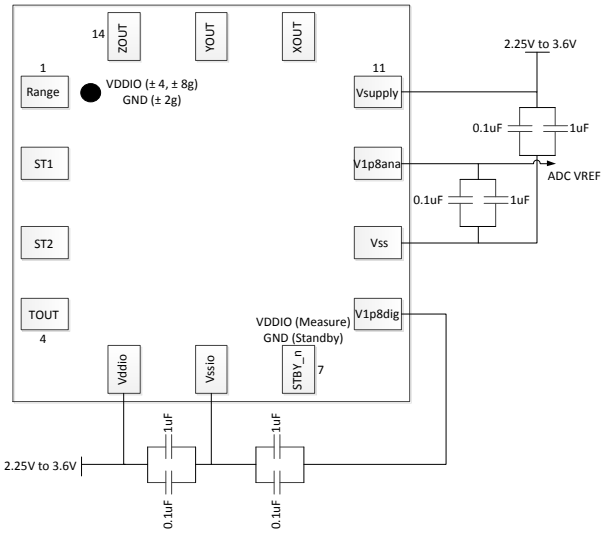

Figure 22. ADXL354 Application Circuit

POWER SEQUENCING

TBD

POWER SUPPLY DESCRIPTION

The ADXL354/ADXL355 has four different power supply domains. The internal analog and digital circuitry operates at 1.8V nominal.

Vsupply: 2.25V-3.6V, input to two low-dropout regulators which generate nominal 1.8V outputs for V1p8ana and V1p8dig.

V1p8ana: All sensor and signal processing circuitry operates in this domain. Offset and sensitivity of the ADXL354 analog output part are ratiometric to this supply voltage. External ADCs should use V1p8ana as the reference voltage. The ADXL355 digital output part includes A/D converters which are ratiometric to V1p8ana, thereby rendering offset and sensitivity insensitive to the value of V1p8ana. V1p8ana may be the output of an internal regulator, or it may be provided externally.

V1p8dig: This is the supply voltage for the internal logic circuitry. A separate LDO regulator is provided to decouple digital supply noise from the analog signal path. V1p8dig may be the output of an internal regulator, or it may be provided externally.

Vddio: Logic 'high' levels are determined by the value of Vddio. On the ADXL354 analog part, Vddio sets the logic high level for the Self-Test pins ST1 and ST2, as well as the STBY_n pin. On the ADXL355 digital part, Vddio sets the logic high level for communications interface ports, as well as the interrupt and DRDY outputs.

The LDO regulators are operational when Vsupply is between 2.25V and 3.6V. V1p8ana and V1p8dig are the regulator outputs in this mode. Alternatively, when Vsupply is tied to Vss, V1p8ana and V1p8dig are supply voltage inputs, with a range of 1.62V-1.98V.

OVER-RANGE PROTECTION

In order to avoid electrostatic capture of the proof-mass when the accelerometer is subjected to input acceleration beyond its full-scale range, all of the sensor drive clocks are turned off for 0.5ms. In the $\pm 2g$ range setting, the over-range protection is activated for input signals beyond $\pm 8g$ ($\pm 25\%$) and for the $\pm 4g$ and $\pm 8g$ ranges the threshold corresponds to $\pm 16g$ ($\pm 25\%$).

SELF TEST

The ADXL354 and ADXL355 incorporate a self-test feature that effectively tests their mechanical and electronic systems simultaneously. In ADXL354, the self-test mode can be invoked by driving the ST1 pin to V_{DDIO}. Then driving the ST2 pin to V_{DDIO} applies an electrostatic force to the mechanical sensor and induces a change in output in response to the force. The self-test delta (or response) is the difference in output voltages between when ST2 is high and ST2 is low, both when ST1 is asserted. After the self-test measurement is complete, bringing both pins low will resume normal operation.

The self-test operation is similar in ADXL355 except ST1 and ST2 can be accessed through the SELF TEST (0x2E) register.

The self-test feature is designed to reject externally applied acceleration and only respond to the self-test force. This allows for an accurate measurement of self-test even in the presence of external mechanical noise.

FILTER

TBD

Table 9. Digital Filter Group Delay

	Delay				Atten.
ODR	SDM cycles	ODR cycles	Theory	msec	@ODR/4 (db)
4000	161	2.52	2.50	0.63	-3.44
2000	257	2.00	2.00	1.00	-2.21
1000	455	1.78	1.75	1.78	-1.92
500	836	1.63	1.63	3.26	-1.83
250	1605	1.57	1.56	6.27	-1.83
125	3160	1.54	1.53	12.34	-1.83
63	6190	1.51	1.52	24.18	-1.83
31	12184	1.49	1.51	47.59	-1.83
16	24640	1.50	1.50	96.25	-1.83
8	48532	1.48	1.50	189.58	-1.83
4	98383	1.50	1.50	384.31	-1.83
With Interpolator					
64xODR					
256000	225	3.51661	3.50	0.88	-6.18
128000	386	3.0126	3.00	1.51	-4.93
64000	705	2.752	2.75	2.75	-4.66
32000	1349	2.63459	2.63	5.27	-4.58
16000	2639	2.57732	2.56	10.31	-4.55
8000	5217	2.54725	2.53	20.38	-4.55
4000	10373	2.53257	2.52	40.52	-4.55
2000	20681	2.52452	2.51	80.78	-4.55
1000	41295	2.52045	2.50	161.31	-4.55
500	82556	2.5194	2.50	322.48	-4.55
250	164963	2.51714	2.50	644.39	-4.55

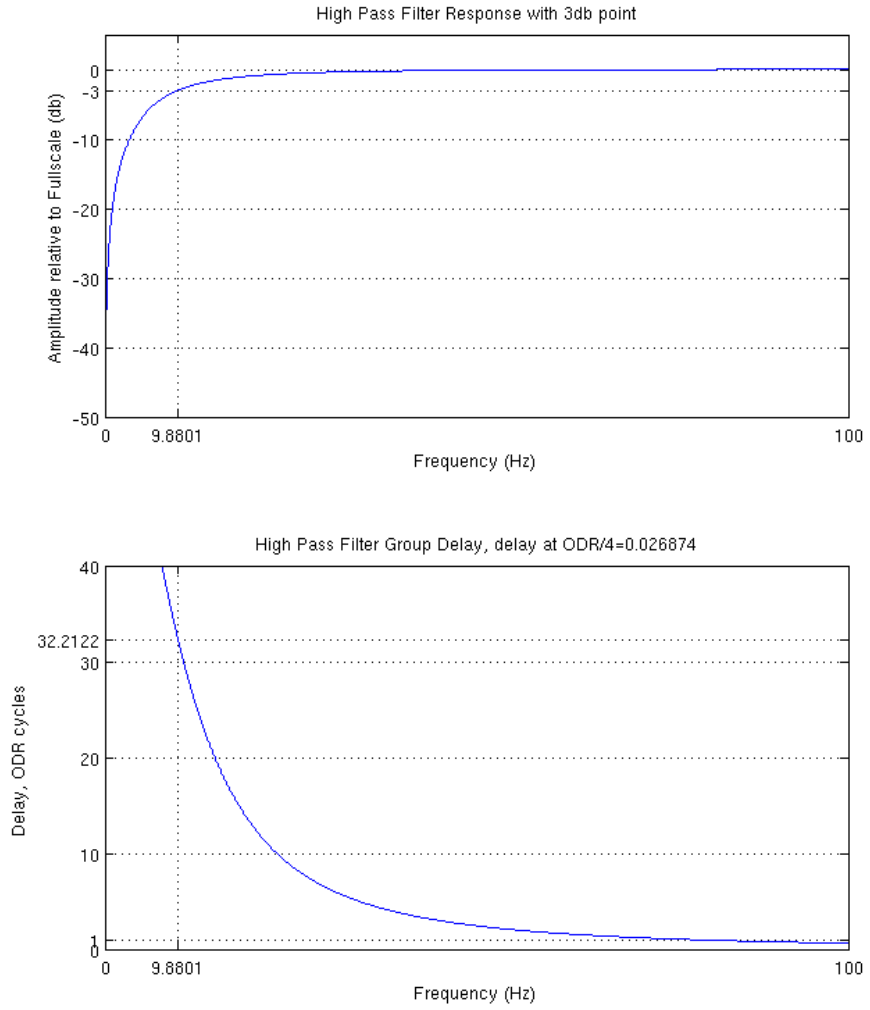

Figure 23 Simulated frequency response of high pass filter with 10Hz cut-off frequency

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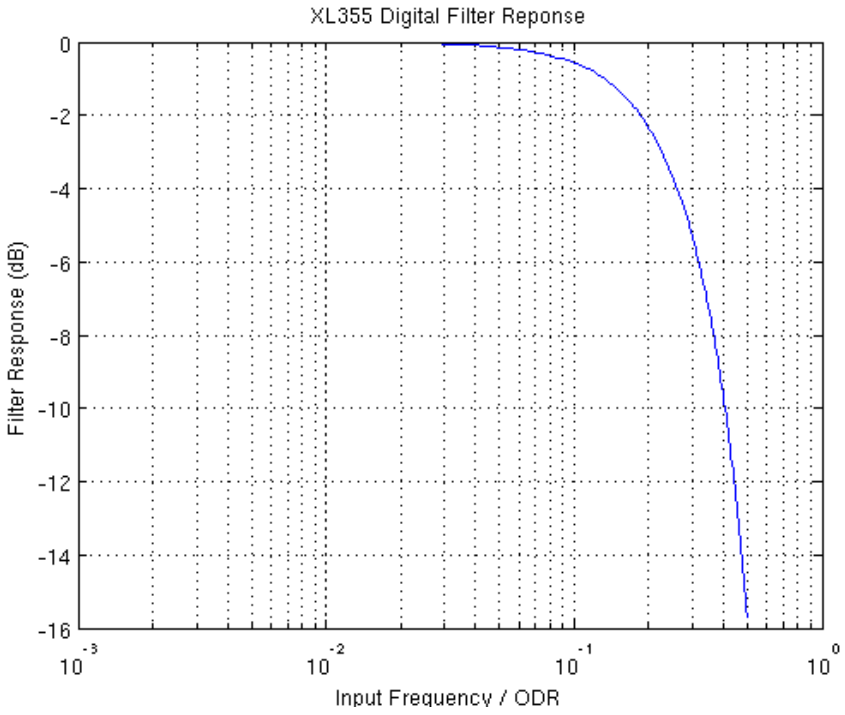

Figure 24 Simulated frequency response of low pass CIC filter with 1kHz corner frequency

SERIAL COMMUNICATION

The four wire serial interface is designed to communicate in either the SPI or I2C protocol. It will affectively auto-detect the format being used, requiring no configuration control to select the format.

SPI PROTOCOL

Wire the ADXL355 for SPI communication as shown in the connection diagram in Figure 25. The SPI protocol is summarized in Figure 26. The timing scheme follows clock polarity (CPOL) = 0 and clock phase (CPHA) = 0. The SPI clock speed can range from 100 kHz to 10 MHz.

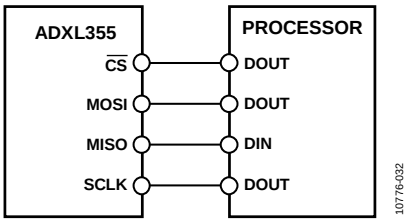

Figure 25. 4-Wire SPI Connection

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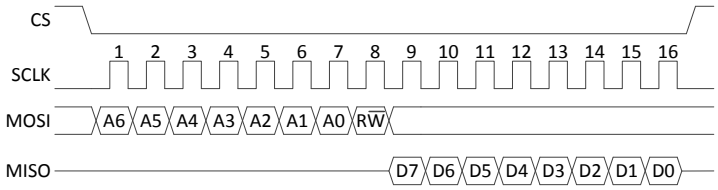
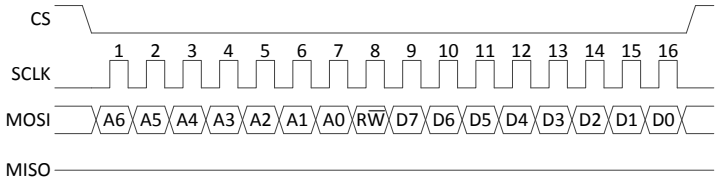
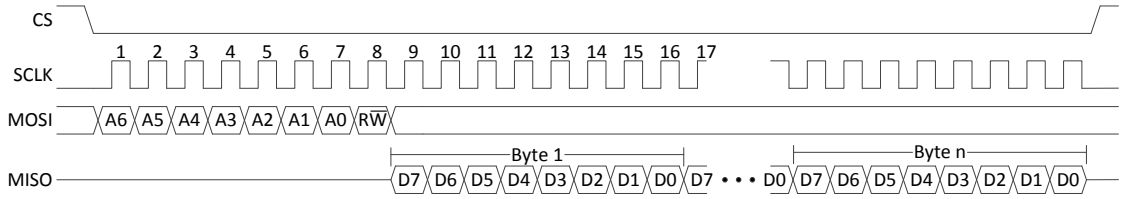


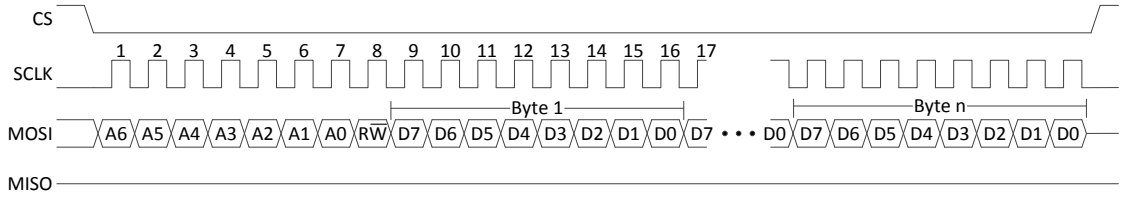
Single Byte Read



Single Byte write



Multi-byte Read



Multi-byte Write

Figure 26: SPI Timing Diagram

I2C PROTOCOL

The I2C protocol is summarized Figure 27. The I2C interface can be used on most buses operating in I2C "Standard mode" (100kHz), "Fast mode" (400kHz), "Fast mode plus" (1MHz), and "High-speed mode" (3.4MHz). The ADXL355 I2C device ID is as follows:
ASEL (pin) = 0, device ID = 7'h1D
ASEL (pin) = 1, device ID = 7'h53

READING ACCELERATION OR TEMPERATURE DATA FROM THE INTERFACE

Acceleration data is left justified and with a register address order of most significant data to least significant data. This allows the user to use multi-byte transfers and to take only as much data as he is interested in, either 8 bits, 16 bits, or 20 bits plus marker. Temperature data is 12-bits unsigned, right-justified. The data in XDATA, YDATA, ZDATA, is always the most recent available. It is not guaranteed that XDATA, YDATA, and ZDATA will form a "set" corresponding to one sample point in time. This data set continuity is instead controlled by the routine used to retrieve the data from the device. If data transfers are initiated when DATA_RDY goes high and completed in a time approximately equal to 1/ODR, then the XDATA, YDATA, ZDATA will apply to the same dataset.

For multi-byte read or write transactions through either serial interface the internal register address will auto-increment. When the top of the register address range, 0x3FF, is reached the auto-increment will stop and not wrap back to the 0x00 address.

The address auto-increment function is disabled when the FIFO address is used. This is so that data can be read continuously from the FIFO as a multi-byte transaction. In cases where the starting address of a multi-byte transaction is less than the FIFO address, the address will auto-increment until the FIFO address is reached and then it will stop at the FIFO address.

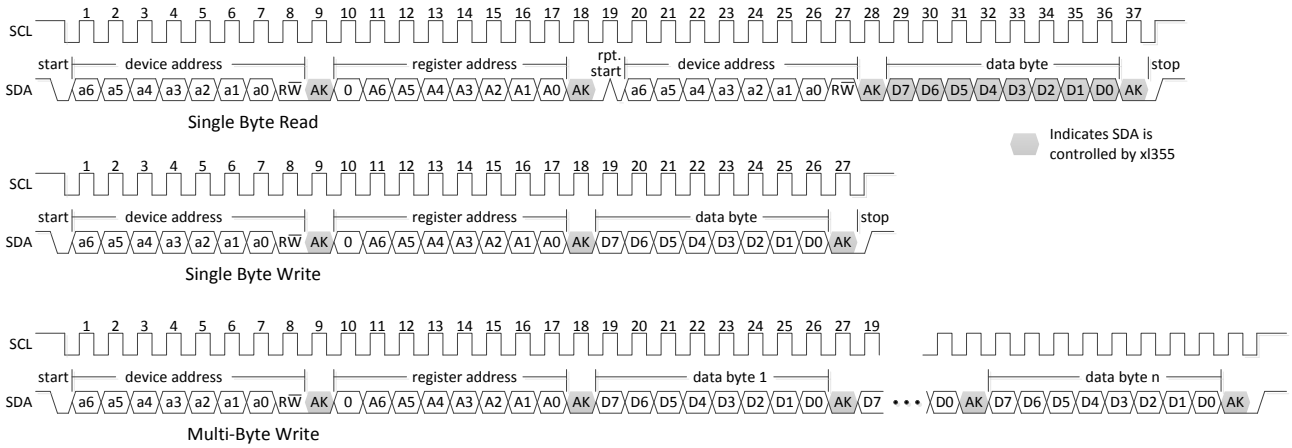


Figure 27. I2C Timing Diagram

FIFO

FIFO operates in a stream mode, that is, when the FIFO overruns new data over-writes the oldest data in the FIFO. A read from the FIFO address guarantees that the three bytes associated with the acceleration measurement on an axis all pertain to the same measurement. It is ensured that the FIFO never over-runs and data is always taken out in sets (multiples of 3 data points).

There are 96 21-bit locations in the FIFO. Each location contains 20-bits of data and a marker bit for X-axis data. A single-byte read from the FIFO address will "pop" one location from the FIFO. A multi-byte read to the FIFO location will pop the FIFO on the read of the first byte and every third byte read thereafter.

Data is organized in the FIFO as shown in Figure 28. The acceleration data is 2's complement 20-bit data. The two LSBs read on the interface are inserted by the FIFO control logic. Bit 1 is an indicator that an attempt was made to read an empty FIFO, and the data is not valid acceleration data. Bit 0 is a "marker" bit to identify the X-axis, which allows a customer to verify that he is reading FIFO data correctly. An acceleration data point for a given axis occupies one FIFO location.

The read pointer (rd_ptr) points to the oldest stored data that has not already been read from the interface. There are no physical X-, Y-, Z- acceleration data registers. This data also comes directly from the most recent data set in the FIFO, which is pointed to by the Z pointer (z ptr).

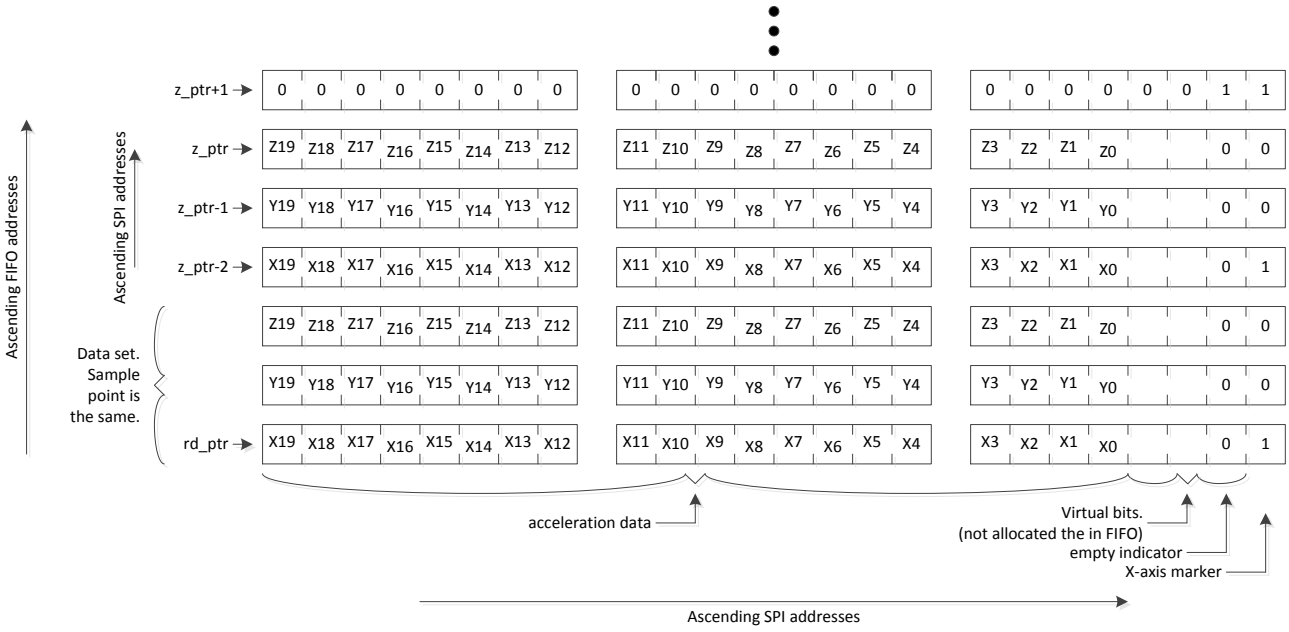


Figure 28. FIFO Data Organization

INTERRUPTS

The STATUS register (0x04) contains five individual bits, four of which can be mapped to either the INT1 pin, the INT2 pin, or both. The polarity of the interrupt, active high or active low, is also selectable via the INT_POL bit in the RANGE (0x2C) register. In general the status register clears when it's read, but this is not the case if the condition which caused the interrupt persists after the read of the register. The definition of "persist" varies slightly in each case, but is described in the following sections. The DRDY pin is similar to an interrupt pin but clears very differently. This case is also described.

DATA_RDY

DATA_RDY is set when new acceleration data is available to the interface. It is cleared on read of the status register. It will not be set again until acceleration data that is newer than the status register read is available.

Special logic was added to the clear of the DATA_RDY bit to cover the corner case where new data arrives during the read of the status register. In which case the data ready condition could be missed completely. This logic results in a delay of the clearing of DATA_RDY of up to four 512 kHz cycles.

FIFO_FULL

FIFO_FULL is set when the entries in the FIFO is equal to the setting of FIFO_SAMPLES. It will clear:

1. If the entries in the FIFO falls below FIFO_SAMPLES. This can only be the case if sufficient data is read from the FIFO.
2. On a read of the status register, but only if the entries in the FIFO is less than FIFO_SAMPLES.

FIFO_OVR

FIFO_OVR is set when the FIFO is so far over range that data has been lost. The specified size of the FIFO is 96 locations. There is an additional three location buffer to compensate for delays in the synchronization of the clock domains. It is only when there is an attempt to write past this 99 location limit that FIFO_OVR is set.

FIFO_OVR is cleared by a read of the status register. It is not set again until data is lost subsequent to this data register read.

ACTIVITY

ACTIVITY will be set when the measured acceleration on any axis is above ACT_THRESH for ACT_COUNT consecutive measurements. An over threshold condition can shift from one axis to another on successive measurements and will still be counted toward the consecutive ACT_COUNT.

ACTIVITY is cleared on read of the status register, but will be set again at the end of the next measurement if the ACTIVITY conditions are still satisfied.

NVM_BUSY

NVM_BUSY indicates that the NVM controller is busy with either refreshing the shadow registers, programming the fuses, or running BIST and it cannot generate an interrupt.

NVM_BUSY is cleared on a status register read that occurs after the NVM is no longer busy.

DRDY

DRDY is not a status register bit, but is instead a pin that behaves similar to an unmaskable interrupt. DRDY is set when new acceleration data is available to the interface. It is cleared:

1. On a read of the FIFO.
2. On a read of XDATA, YDATA, or ZDATA.
3. By an auto-clear function that occurs approximately halfway between output acceleration data sets.

DRDY is always active high. It is not affected by the INT_POL bit field. In EXT_SYNC modes the first few DRDY pulses after initial synchronization can be lost or corrupted. The length of this potential corruption is less than the group delay.

EXTERNAL SYNC AND INTERPOLATION

The three proposed external SYNC, interpolation options are shown in Figure 6. For clarity, the clock frequencies and delays are drawn to scale.

"Internal ODR" is the output rate of the decimation filter.

Rev PrD

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"ADC mod. clk. Is the analog modulator clock rate. The (4*64)X ODR example is for a 4000Hz ODR. For other ODR_LPF settings the SYNC frequency approximates the ODR. The relationship to the oscillator clock is modified to: OSC = (4000/ODR)*(4*64)*SYNC. Oscillator clock frequency of 1.024MHz should be used. The oscillator clock must be provided on INT2 pin (Pin 13) and the external SYNC on DRDY pin (Pin 14) as highlighted in Table 8.

Group delay is the digital filter delay from the input to the ADC until data is available at the interface. It is detailed in 9. This delay is the largest component of the total delay from sensor to serial interface. Figure XX and Figure XX show simulated filter response for the high pass filter with 10Hz cut-off and low pass filter with 1kHz corner.

DRDY is an optional output pin.

SYNC is an optional input pin.

Table 8. Multiplexing of INT2_XOUT and DRDY_ZOUT

Register Bit Fields			Pins		
EXT_ CLK	EXT_ SYNC [1:0]	INT2_EN [3:0]	INT2 Pin 13	DRDY Pin 14	Comments
0	00	0000	LO	DRDY	Internal Sync
0	00	not 0000	INT2	DRDY	
1	00	0000	EXT_CLK	DRDY	
1	00	not 0000[2]	EXT_CLK	DRDY	
0	01	0000	DRDY	SYNC	These options will reset the digital filters on every SYNC pulse and are not recommended.
0	01[1]	not 0000	INT2	SYNC	
1	01[1]	0000	EXT_CLK	SYNC	External Sync, no interpolation filter, data on RDY. Data represents a sample point "group_delay" earlier in time.
1	01[1]	not 0000[2]	EXT_CLK	SYNC	
0	10	0000	DRDY	SYNC	External Sync, interpolation filter, data on RDY or DRDY. Data sampled "group_delay" earlier in time.
0	10[1]	not 0000	INT2	SYNC	
1	10[1]	0000	EXT_CLK	SYNC	
1	10[1]	not 0000	EXT_CLK	SYNC	

Notes

1 No DRDY

2 No INT2, even though it is enabled.

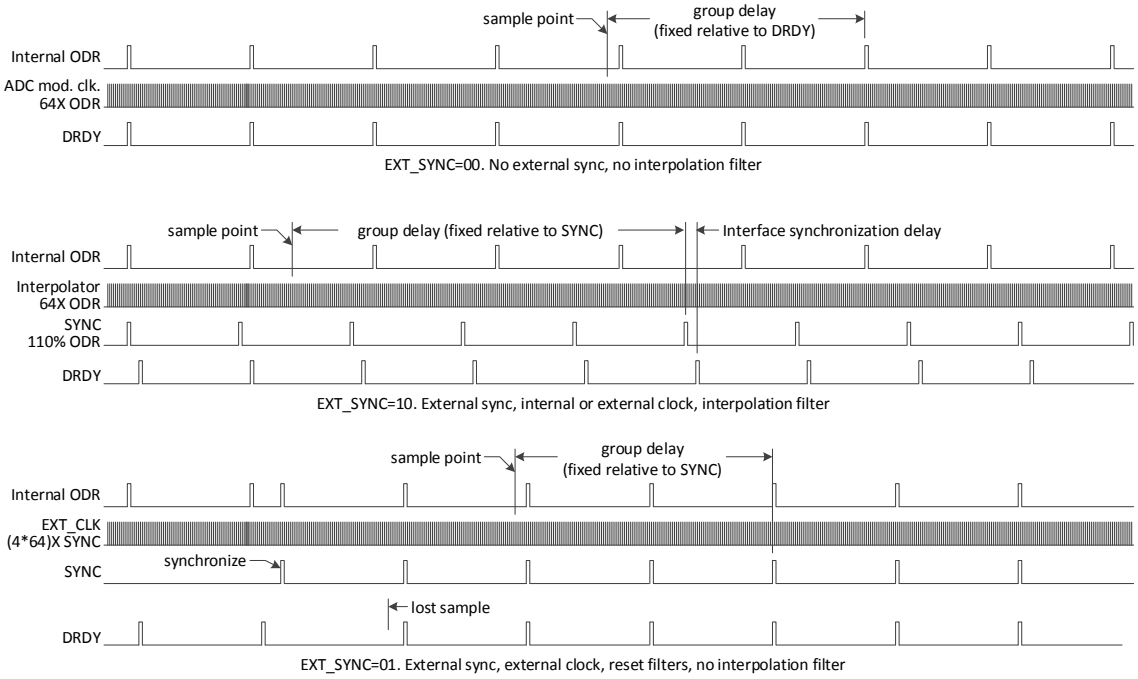

Figure 12. External Synchronization Options.

EXT_SYNC=00. No External SYNC or Interpolation.

This option is shown as a baseline. This example is for ODR_LPF=0000, the default 4000Hz output rate option. The group delay is shown in **Error! Reference source not found.**.

EXT_SYNC=10. External SYNC with Interpolation.

In this case the internal decimation filter runs exactly as it does in the baseline case, but the user has access to data points between the normal decimation filter outputs. The time resolution of these intermediate points is 1/64*ODR period. The interface delay shown in Table 10.

Table 10. EXT_SYNC=10 DRDY Delay

ODR_LPF	Delay (osc cycles)
0h	8
1h	10
2h	14
3h	22
4h	38
5h	70
6h	134
7h	262
8h	1031
9h	2054
10h	4102

EXT_SYNC=01. External SYNC with filter synchronization and no interpolation.

With this option the external SYNC is used to synchronize the internal decimation filter such that data is available at the optimum time. There is an initial synchronization of this mode that corrupts the first output data samples that are within one group delay of the EXT_SYNC (from 1-3). If the restrictions below are

respected, this corruption happens only once when the SYNC stream begins.

Special restrictions when using this mode are:

1. An external clock (EXT_CLK) must be provided as well as an external SYNC.
2. The frequency of EXT_CLK must be exactly 4*64x the frequency of SYNC.
3. The width of SYNC must be a minimum of 4 EXT_CLK periods.
4. The phase of SYNC must meet an approximate 25nsec setup time to EXT_CLK rising edge.

Note that if EXT_SYNC mode is used and no SYNC is provided, the device will run on its own synchronization. Similarly, after synchronization the device will continue to run synchronized to the last SYNC pulse it received. This means that EXT_SYNC=01 mode can be used with only a single synchronization pulse.

ADXL355 REGISTER MAP

Note: While configuring the ADXL355 in an application, all configuration registers must be programmed before enabling measure mode in POWER_CTL register. When the part is in measure mode, only the following configurations can be changed: (i) HPF_CORNER bits in FILTER register, (ii) INT_MAP register, (iii) ST1 and ST2 fields in SELF_TEST register, (iv) RESET register.

Table 11. ADXL355 Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	DEVID_AD	[7:0]	DEVID_AD								0xAD	R
0x01	DEVID_MST	[7:0]	DEVID_MST								0x1D	R
0x02	PARTID	[7:0]	PARTID								0xED	R
0x03	REVID	[7:0]	REVID								0x00	R
0x04	STATUS	[7:0]	RESERVED			NVM_BUSY	ACTIVITY	FIFO_OVR	FIFO_FULL	DATA_RDY	0x00	R
0x05	FIFO_ENTRIES	[7:0]	RESERVED	FIFO_ENTRIES							0x00	R
0x06	TEMP2	[7:0]	RESERVED				TEMPERATURE[11:8]				0x00	R
0x07	TEMP1	[7:0]	TEMPERATURE[7:0]								0x00	R
0x08	XDATA3	[7:0]	XDATA[19:12]								0x00	R
0x09	XDATA2	[7:0]	XDATA[11:4]								0x00	R
0x0A	XDATA1	[7:0]	XDATA[3:0]				RESERVED				0x00	R
0x0B	YDATA3	[7:0]	YDATA[19:12]								0x00	R
0x0C	YDATA2	[7:0]	YDATA[11:4]								0x00	R
0x0D	YDATA1	[7:0]	YDATA[3:0]				RESERVED				0x00	R
0x0E	ZDATA3	[7:0]	ZDATA[19:12]								0x00	R
0x0F	ZDATA2	[7:0]	ZDATA[11:4]								0x00	R
0x10	ZDATA1	[7:0]	ZDATA[3:0]				RESERVED				0x00	R
0x11	FIFO_DATA	[7:0]	FIFO_DATA								0x00	R
0x1E	OFFSET_X_H	[7:0]	OFFSET_X[15:8]								0x00	R/W
0x1F	OFFSET_X_L	[7:0]	OFFSET_X[7:0]								0x00	R/W
0x20	OFFSET_Y_H	[7:0]	OFFSET_Y[15:8]								0x00	R/W
0x21	OFFSET_Y_L	[7:0]	OFFSET_Y[7:0]								0x00	R/W
0x22	OFFSET_Z_H	[7:0]	OFFSET_Z[15:8]								0x00	R/W
0x23	OFFSET_Z_L	[7:0]	OFFSET_Z[7:0]								0x00	R/W
0x24	ACT_EN	[7:0]	RESERVED					ACT_Z	ACT_Y	ACT_X	0x00	R/W
0x25	ACT_THRESH_H	[7:0]	ACT_THRESH[15:8]								0x00	R/W
0x26	ACT_THRESH_L	[7:0]	ACT_THRESH[7:0]								0x00	R/W
0x27	ACT_COUNT	[7:0]	ACT_COUNT								0x01	R/W
0x28	FILTER	[7:0]	RESERVED	HPF_CORNER			ODR_LPF				0x00	R/W
0x29	FIFO_SAMPLES	[7:0]	RESERVED	FIFO_SAMPLES							0x60	R/W
0x2A	INT_MAP	[7:0]	ACT_EN2	OVR_EN2	FULL_EN2	RDY_EN2	ACT_EN1	OVR_EN1	FULL_EN1	RDY_EN1	0x00	R/W
0x2B	SYNC	[7:0]	RESERVED					EXT_CLK	EXT_SYNC		0x00	R/W
0x2C	RANGE	[7:0]	I2C_HS	INT_POL	RESERVED				RANGE		0x81	R/W
0x2D	POWER_CTL	[7:0]	RESERVED					DRDY_OFF	TEMP_OFF	STANDBY	0x01	R/W

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Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2E	SELF_TEST	[7:0]	RESERVED						ST2	ST1	0x00	R/W
0x2F	RESET	[7:0]	RESET								0x00	W

REGISTER DEFINITIONS

This section describes the functions of the ADXL355 registers. The ADXL355 powers up with default register values as shown in the Reset column of Table .

ANALOG DEVICES ID REGISTER

Address: 0x00, Reset: 0xAD, Name: DEVID_AD

This register contains the Analog Devices ID, 0xAD.

Table 12. Bit descriptions for DEVID_AD

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVID_AD		Analog Devices ID, 0xAD	0xAD	R

ANALOG DEVICES MEMS ID REGISTER

Address: 0x01, Reset: 0x1D, Name: DEVID_MST

This register contains the Analog Devices MEMS ID, 0x1D.

Table 13. Bit descriptions for DEVID_MST

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVID_MST		Analog Devices MEMS ID, 0x1D	0x1D	R

DEVICE ID REGISTER

Address: 0x02, Reset: 0xED, Name: PARTID

This register contains the device ID, 0xED (355 octal).

Table 14. Bit descriptions for PARTID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PARTID		Device ID, 0xED (355 Octal)	0xED	R

PRODUCT REVISION ID REGISTER

Address: 0x03, Reset: 0x00, Name: REVID

This register contains the product revision ID, beginning with 0x00 and incrementing for each subsequent revision.

Table 5. Bit descriptions for REVID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	REVID		Mask revision	0x0	R

STATUS REGISTER

Address: 0x04, Reset: 0x00, Name: STATUS

This register includes the following bits that describe various conditions of the ADXL355.

Table 66. Bit descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved.	0x0	R
6	Reserved		Reserved.	0x0	R
5	Reserved		Reserved.	0x0	R
4	NVM_BUSY		NVM is busy with either refresh, programming or BIST.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
3	ACTIVITY		Activity as defined in the THRESH_ACT and COUNT_ACT registers has been detected.	0x0	R
2	FIFO_OVR		FIFO has overrun and the oldest data has been lost.	0x0	R
1	FIFO_FULL		FIFO watermark has been reached.	0x0	R
0	DATA_RDY		A complete X, Y and Z measurement has been made and results can be read.	0x0	R

FIFO ENTRIES REGISTERS

Address: 0x05, Reset: 0x00, Name: FIFO_ENTRIES

These registers indicate the number of valid data samples present in the FIFO buffer. This number ranges from 0 to 96.

Table 17. Bit descriptions for FIFO_ENTRIES

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved	0x0	R
[6:0]	FIFO_ENTRIES		Number of data samples stored in the FIFO.	0x0	R

TEMPERATURE DATA REGISTERS

Address: 0x06, Reset: 0x00, Name: TEMP2

These two registers contain the uncalibrated temperature data. The nominal intercept is 1852 LSB at 25 °C and the nominal slope is -9.05LSB/°C. TEMP2 contains the 4 most significant bits (MSBs), and TEMP1 contains the 8 least significant bits (LSBs) of the 12-bit value.

Table 18. Bit descriptions for TEMP2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED				
[3:0]	TEMPERATURE[11:8]		Uncalibrated temperature data.	0x0	R

Address: 0x07, Reset: 0x00, Name: TEMP1

Table 79. Bit descriptions for TEMP1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMPERATURE[7:0]		Uncalibrated temperature data.	0x0	R

X-AXIS DATA REGISTERS

Address: 0x08, Reset: 0x00, Name: XDATA3

These three registers contain the X-axis acceleration data. Data is left-justified and formatted as two's complement.

Table 20. Bit descriptions for XDATA3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	XDATA[19:12]		X-axis data.	0x0	R

Address: 0x09, Reset: 0x00, Name: XDATA2

Table 21. Bit descriptions for XDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	XDATA[11:4]		X-axis data.	0x0	R

Address: 0x0A, Reset: 0x00, Name: XDATA1

Table 22. Bit descriptions for XDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	XDATA[3:0]		X-axis data.	0x0	R
[3:0]	Reserved		Reserved.	0x0	R

Y-AXIS DATA REGISTERS

Address: 0x0B, Reset: 0x00, Name: YDATA3

These three registers contain the Y-axis acceleration data. Data is left-justified and formatted as two's complement.

Table 23. Bit descriptions for YDATA3

Bits		Bit Name	Settings	Description	Reset	Access
[7:0]		YDATA[19:12]		Y-axis data.	0x0	R

Address: 0x0C, Reset: 0x00, Name: YDATA2

Table 84. Bit descriptions for YDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	YDATA[11:4]		Y-axis data.	0x0	R

Address: 0x0D, Reset: 0x00, Name: YDATA1

Table 25. Bit descriptions for YDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	YDATA[3:0]		Y-axis data.	0x0	R
[3:0]	Reserved		Reserved.	0x0	R

Z-AXIS DATA REGISTERS

Address: 0x0E, Reset: 0x00, Name: ZDATA3

These three registers contain the Z-axis acceleration data. Data is left-justified and formatted as two's complement.

Table 26. Bit descriptions for ZDATA3

Bits			Bit Name	Settings	Description	Reset	Access
[7:0]			ZDATA[19:12]		Z-axis data.	0x0	R

Address: 0x0F, Reset: 0x00, Name: ZDATA2

Table 27. Bit descriptions for ZDATA2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ZDATA[11:4]		Z-axis data.	0x0	R

Address: 0x10, Reset: 0x00, Name: ZDATA1

Table 28. Bit descriptions for ZDATA1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	ZDATA[3:0]		Z-axis data.	0x0	R
[3:0]	Reserved		Reserved.	0x0	R

FIFO ACCESS REGISTER

Address: 0x11, Reset: 0x00, Name: FIFO_DATA

Read this register to access data stored in the FIFO.

Table 29. Bit descriptions for FIFO_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FIFO_DATA		FIFO data is formatted to 24 bits, 3 bytes, Most significant byte first. A read to this address "pops" an effective 3 equal byte word of axis data from the FIFO. Two subsequent reads or a multi-byte read completes the transaction of this data onto the interface. Continued reading or a sustained multi-byte read of this field will continue to pop the FIFO every third byte. Multi-byte reads to this address will not increment the address pointer. If this address is read due to an auto-increment from the previous address it will not pop the FIFO instead it will return zeros and increment on to the next address.	0x0	R

X-AXIS OFFSET TRIM REGISTERS

Address: 0x1E, Reset: 0x00, Name: OFFSET_X_H

Table 30. Bit descriptions for OFFSET_X_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_X[15:8]		Offset added to X-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_X[15:0] matches the significance of XDATA[19:4].	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: OFFSET_X_L

Table 31. Bit descriptions for OFFSET_X_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_X[7:0]		Offset added to X-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_X[15:0] matches the significance of XDATA[19:4].	0x0	R/W

Y-AXIS OFFSET TRIM REGISTERS

Address: 0x20, Reset: 0x00, Name: OFFSET_Y_H

Table 32. Bit descriptions for OFFSET_Y_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Y[15:8]		Offset added to Y-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_Y[15:0] matches the significance of YDATA[19:4].	0x0	R/W

Address: 0x21, Reset: 0x00, Name: OFFSET_Y_L

Table 33. Bit descriptions for OFFSET_Y_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Y[7:0]		Offset added to Y-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_Y[15:0] matches the significance of YDATA[19:4].	0x0	R/W

Z-AXIS OFFSET TRIM REGISTERS

Address: 0x22, Reset: 0x00, Name: OFFSET_Z_H

Table 34. Bit descriptions for OFFSET_Z_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Z[15:8]		Offset added to Z-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_Z[15:0] matches the significance of ZDATA[19:4].	0x0	R/W

Address: 0x23, Reset: 0x00, Name: OFFSET_Z_L

Table 95. Bit descriptions for OFFSET_Z_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	OFFSET_Z[7:0]		Offset added to Z-axis data after all other signal processing. Data is in two's complement format. The significance of OFFSET_Z[15:0] matches the significance of ZDATA[19:4].	0x0	R/W

ACTIVITY ENABLE REGISTER

Address: 0x24, Reset: 0x00, Name: ACT_EN

Table 36. Bit descriptions for ACT_EN

Bits		Bit Name	Settings	Description	Reset	Access
[7:3]		RESERVED		Reserved.	0x0	R
2		ACT_Z		Z-axis data is a component of the activity detection algorithm.	0x0	R/W
1		ACT_Y		Y-axis data is a component of the activity detection algorithm.	0x0	R/W
0		ACT_X		X-axis data is a component of the activity detection algorithm.	0x0	R/W

ACTIVITY THRESHOLD REGISTERS

Address: 0x25, Reset: 0x00, Name: ACT_THRESH_H

Table 37. Bit descriptions for ACT_THRESH_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_THRESH[15:8]		Threshold for activity detection. Acceleration magnitude must be above ACT_THRESH to trigger the activity counter. ACT_THRESH is an unsigned magnitude. The significance of ACT_TRESH[15:0] matches the significance of X-, Y-, ZDATA[18:3].	0x0	R/W

Address: 0x26, Reset: 0x00, Name: ACT_THRESH_L

Table 38. Bit descriptions for THRESH_ACT_X_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_THRESH[7:0]		Threshold for activity detection. Acceleration magnitude must be above ACT_THRESH to trigger the activity counter. ACT_THRESH is an unsigned magnitude. The significance of ACT_TRESH[15:0] matches the significance of X-, Y-, ZDATA[18:3].	0x0	R/W

ACTIVITY COUNT REGISTER

Address: 0x27, Reset: 0x00, Name: ACT_COUNT

Table 39. Bit descriptions for ACT_COUNT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ACT_COUNT		Number of consecutive events above threshold required to detect activity	0x1	R/W

FILTER SETTINGS REGISTER

Address: 0x28, Reset: 0x00, Name: FILTER

Use this register to specify parameters for the internal high-pass and low-pass filters.

Table 40. Bit descriptions for FILTER

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	HPF_CORNER		-3db filter corner for the 1st order high-pass filter relative to the output data rate (ODR).	0x0	R/W
		000	No high pass filtering.		
		001	24.700E-4 * ODR		
		010	6.2084E-4 * ODR		
		011	1.5545E-4 * ODR		
		100	0.3862E-4 * ODR		
		101	0.0954E-4 * ODR		
		110	0.0238E-4 * ODR		
[3:0]	ODR_LPF		Output data rate and low-pass filter corner	0x0	R/W
		0000	4000Hz, 1000Hz.		
		0001	2000Hz, 500Hz.		
		0010	1000Hz, 250Hz.		
		0011	500Hz, 125Hz.		
		0100	250Hz, 62.5Hz.		
		0101	125Hz, 31.25Hz.		
		0110	62.5Hz, 15.625Hz.		
		0111	31.25Hz, 7.813Hz.		
		1000	15.625Hz, 3.906Hz.		
		1001	7.813Hz, 1.953Hz.		
		1010	3.906Hz, 0.977Hz.		

FIFO SAMPLES REGISTER

Address: 0x29, Reset: 0x60, Name: FIFO_SAMPLES

Use the FIFO_SAMPLES value to specify the number of samples to store in the FIFO. The default value of this register is 0x60 to avoid triggering the FIFO watermark interrupt.

Table 41. Bit descriptions for FIFO_SAMPLES

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[6:0]	FIFO_SAMPLES		Watermark number of samples stored in the FIFO that triggers a FIFO_FULL condition. Values range from 1 to 96.	0x60	R/W

INTERRUPT PIN FUNCTION MAP REGISTER

Address: 0x2A, Reset: 0x00, Name: INT_MAP

The INT_MAP register configures the interrupt pins. Bits[7:0] select which function(s) generate an interrupt on the INT1 and INT2 pins. If its corresponding bit is set to 1, the function generates an interrupt on the interrupt pins.

Table 42. Bit descriptions for INT_MAP

Bits	Bit Name	Settings	Description	Reset	Access
7	ACT_EN2		ACTIVITY interrupt enable onto INT2	0x0	R/W
6	OVR_EN2		FIFO_OVR interrupt enable onto INT2	0x0	R/W
5	FULL_EN2		FIFO_FULL interrupt enable onto INT2	0x0	R/W
4	RDY_EN2		DATA_RDY interrupt enable onto INT2	0x0	R/W
3	ACT_EN1		ACTIVITY interrupt enable onto INT1	0x0	R/W
2	OVR_EN1		FIFO_OVR interrupt enable onto INT1	0x0	R/W
1	FULL_EN1		FIFO_FULL interrupt enable onto INT1	0x0	R/W
0	RDY_EN1		DATA_RDY interrupt enable onto INT1	0x0	R/W

DATA SYNCHRONIZATION

Address: 0x2B, Reset: 0x00, Name: SYNC

Use this register to control external timing triggers.

Table 43. Bit descriptions for SYNC

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R
2	EXT_CLK		Enable external clock	0x0	R/W
[1:0]	EXT_SYNC		Enable external SYNC control.	0x0	R/W
		00	Internal SYNC.		
		01	External sync, no interpolation filter. After synchronization, and for EXT_SYNC within spec, DATA_RDY will occur on EXT_SYNC.		
		10	External sync, interpolation filter, next available data indicated by DATA_RDY 14 to 8204 oscillator cycles later (longer delay for higher ODR_LPF setting), Data represents a sample point "group_delay" earlier in time.		
		11	Reserved.		

I2C SPEED, INTERRUPT POLARITY AND RANGE REGISTER

Address: 0x2C, Reset: 0x81, Name: RANGE

Table 44. Bit descriptions for RANGE

Bits	Bit Name	Settings	Description	Reset	Access
7	I2C_HS		I2C speed. 1 = High Speed mode.	0x1	R/W
6	INT_POL		Interrupt polarity.	0x0	R/W
		0	INT1 and INT2 are active low.		
		1	INT1 and INT2 are active high.		
[5:2]	Reserved		Reserved.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	RANGE		Range	0x1	R/W
		01	±2g		
		10	±4g		
		11	±8g		

POWER CONTROL REGISTER

Address: 0x2D, Reset: 0x01, Name: POWER_CTL

Table 45. Bit descriptions for POWER_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	Reserved		Reserved.	0x0	R
2	DRDY_OFF		"1" forces the DRDY output to zero in modes where it would normally signal "data ready".	0x0	R/W
1	TEMP_OFF		"1" disables temperature processing. Temperature processing is also disabled when STANDBY=1.	0x0	R/W
0	STANDBY		1 = standby, 0 = measure. In standby mode the device is in a low power state. The temperature and acceleration data paths are not operating. Digital functions, including FIFO pointers reset. Changes to the configuration setting of the part should be made when STANDBY = 1. An exception is HPF, which can be changed while to part is operating.	0x1	R/W

SELF-TEST REGISTER

Address: 0x2E, Reset: 0x00, Name: SELF_TEST

Refer to the Self-Test section for information on the operation of the self -test feature.

Table 46. Bit descriptions for SELF_TEST

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	Reserved		Reserved.	0x0	R
1	ST2		"1" enables self-test force	0x0	R/W
0	ST1		"1" enables self-test mode	0x0	R/W

RESET REGISTER

Address: 0x2F, Reset: 0x00, Name: RESET

Table 47. Bit descriptions for RESET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RESET		Writing code "0x52" resets the device, similar to a Power-On-Reset.	0x0	W

RECOMMENDED SOLDERING PROFILE

Figure 29 and 45 provide details about the recommended soldering profile.

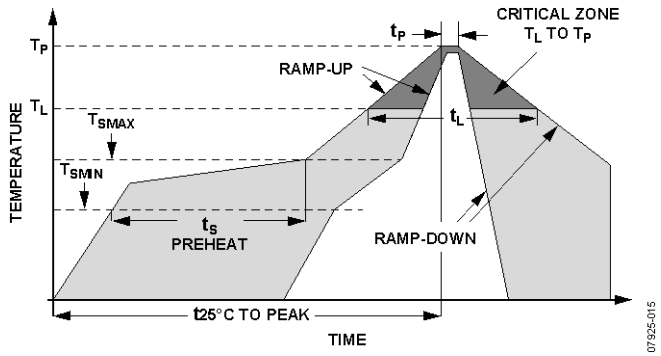

Figure 29. Recommended Soldering Profile

Table 48: Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate from Liquid Temperature (T_L) to Peak Temperature (T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time from T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec max	3°C/sec max
Liquid Temperature (T_L)	183°C	217°C
Time Maintained Above T_L (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time of Actual T_P − 5°C (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 minutes max	8 minutes max

PCB FOOTPRINT PATTERN

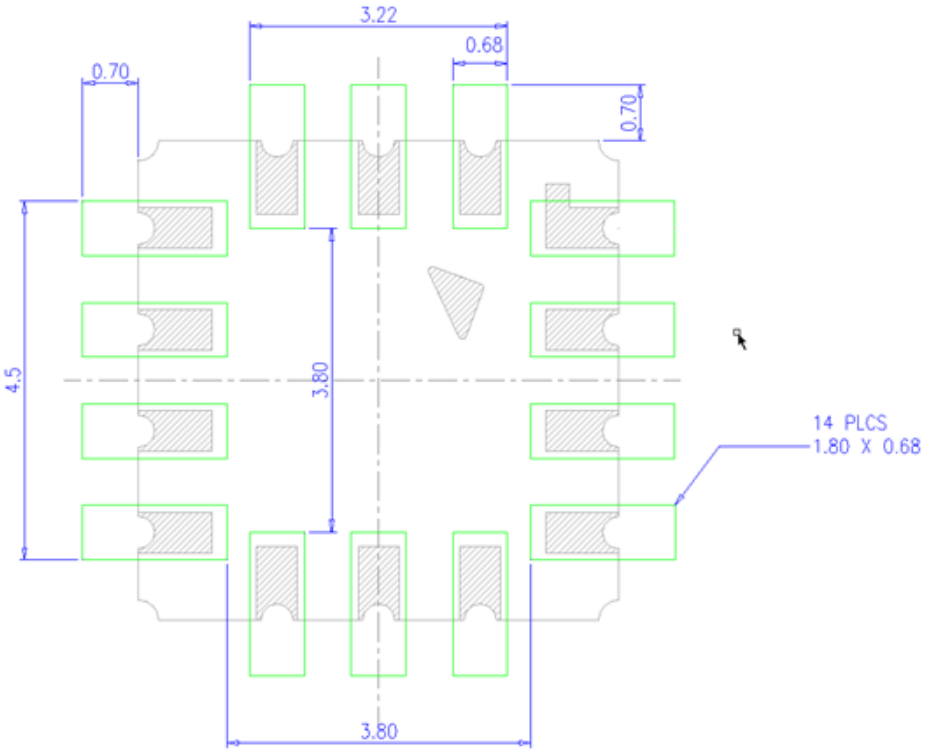

Figure 30. PCB Footprint Pattern and Dimensions (in mm)

OUTLINE DIMENSIONS

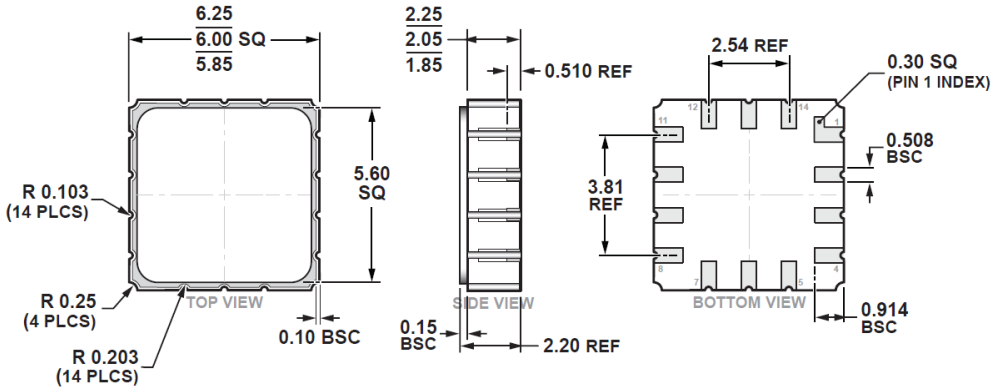

Figure 31: 14-Terminal Ceramic Leadless Chip Carrier (LCC). Dimensions are shown in millimeters.

ORDERING GUIDE

Model	Output Mode	Measurement Range (*g*)	Specified Voltage (V)	Temperature Range	Package Description
ADXL354BEZ	Analog	±2, ±4	3.0	−40°C to +125°C	Ceramic LCC
ADXL354BEZ-RL	Analog	±2, ±4	3.0	−40°C to +125°C	Ceramic LCC
ADXL354BEZ-RL7	Analog	±2, ±4	3.0	−40°C to +125°C	Ceramic LCC
ADXL354CEZ	Analog	±2, ±8	3.0	−40°C to +125°C	Ceramic LCC
ADXL354CEZ-RL	Analog	±2, ±8	3.0	−40°C to +125°C	Ceramic LCC
ADXL354CEZ-RL7	Analog	±2, ±8	3.0	−40°C to +125°C	Ceramic LCC
ADXL355BEZ	Digital	±2, ±4, ±8	3.0	−40°C to +125°C	Ceramic LCC
ADXL355BEZ-RL	Digital	±2, ±4, ±8	3.0	−40°C to +125°C	Ceramic LCC
ADXL355BEZ-RL7	Digital	±2, ±4, ±8	3.0	−40°C to +125°C	Ceramic LCC
EVAL-ADXL354BZ					Evaluation Board
EVAL-ADXL354CZ					Evaluation Board
EVAL-ADXL355Z					Evaluation Board
EVAL-ADXL355Z-M					Analog Devices Inertial Sensor Evaluation System, Includes ADXL355 Satellite
EVAL-ADXL355Z-S					ADXL355 Satellite, Standalone

D07925-0-5/09(0)

ANALOG DEVICES

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